Design and Manufacturing of the SiC-Based Power Supply System for Resistive-Wall-Mode Control in JT-60SA

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***Abstract*— In JT-60SA, the control of resistive-wall-mode (RWM) instabilities will also be realized with a dedicated active control system based on 18 in-vessel sector coils. Each coil will be fed independently by a dedicated fast inverter. Due to the outstanding dynamic performance required, new insulated-gate bipolar transistor modules based on silicon carbide (SiC) have been adopted. Being capable to switch at 30 kHz, these components, together with a very fast control system, allow reaching the required high dynamic performance with the simple and compact H-bridge topology. The RWM-PS will be the first power supply system for fast control of plasma instabilities in fusion experiments adopting SiC semiconductors. This paper gives an overview of the final design of the RWM-PS, with particular emphasis on its special features and the solutions implemented to satisfy the critical requirements. The issues related with the high switching frequency and the peculiar nature of the load will be treated in detail.**

***Index Terms*— Insulated gate bipolar transistors, plasma stability, power supplies, pulsewidth modulated power converters.**

I. Introduction

ONE of the main objectives of JT-60SA, the tokamak under construction in Naka (Japan) [1], is to confine steady-state high-beta plasmas [2]. To reach the desired plasma performance, the control of the instabilities called resistive-wall modes (RWMs) is crucial. To this purpose, besides the combination of an in-vessel passive structure (stabilizing plate) and plasma rotation, a dedicated active control system based on 18 in-vessel sector coils (called RWM control coils, RWM-CC) has been devised [3]. Nowadays, the active control of the plasma instabilities has been implemented in the majority of the existing fusion experiments [4]. However, the peculiarity of the JT-60SA RWM-CC is that they are placed on the plasma side of the stabilizing plate, just behind the tiles of the first wall and around the ports. Therefore, due to the plasma proximity and the low shielding effect of the surrounding passive structures, they can efficiently generate fast magnetic fields if properly driven. The strategy is to succeed in controlling RWMs (which grow exponentially) when their amplitude is still low, so that low magnetic field components and relevant current to produce them are sufficient. As a consequence, the power rating of the power supply system is not so demanding, but at the cost of high dynamic performance. To achieve an effective control and the highest flexibility, each coil will be fed independently by a dedicated converter, which has to follow in real time an arbitrary reference generated by the central MHD controller of JT-60SA. In the following, the term "inverter" will be used to indicate this converter, for clarity.

The required coil current and dynamics have been estimated with VALEN code [5]. The results were a current peak of 275 A, a closed-loop bandwidth of 3 kHz and a latency between reference and output lower than 50 μs [6]. This dynamic performance exceeds the one available from standard industrial products and call for the adoption of innovative solutions. To exploit the simple and compact H-bridge topology, a switching frequency higher than that sustainable by standard silicon insulated-gate bipolar transistors (IGBTs) is necessary; the adoption of new power semiconductors based on silicon carbide (SiC) and a very fast control system have been the key design choices to satisfy the requirements.

To prove the feasibility at reasonable cost of this design, an inverter prototype has been developed in 2014 and fully characterized in 2015–2016. Considering the very satisfactory performance obtained [7], the same inverter design has been confirmed for the final power supply system (called RWM-PS) also. However, some open issues remained on the control section, related to the arbitrary reference and the additional constraints imposed on the output voltage transients. These, together with some thermal upgrades in view of the continuous operation of the full system, have been addressed with the latest developments.

The RWM-PS, now under manufacturing, will be the first power supply system for fast control of plasma instabilities in fusion experiments adopting SiC semiconductors [8]. This paper gives an overview of the final design of the RWM-PS, with particular emphasis on its special features and the solutions adopted to solve the issues related to the

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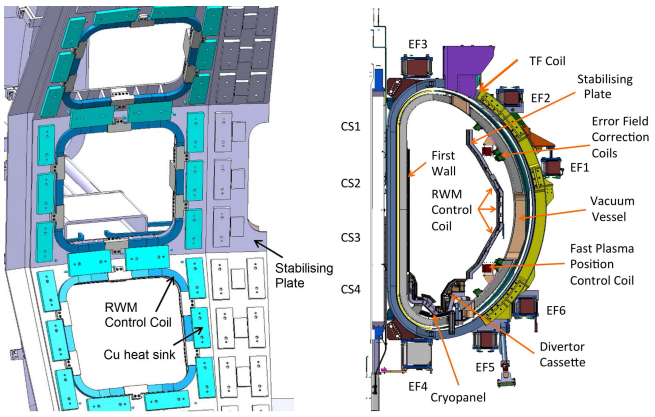

Fig. 1. Typical set of three RWM-CC at the same toroidal angle (carbon tiles not shown) (left). Cross section of JT-60SA (right).

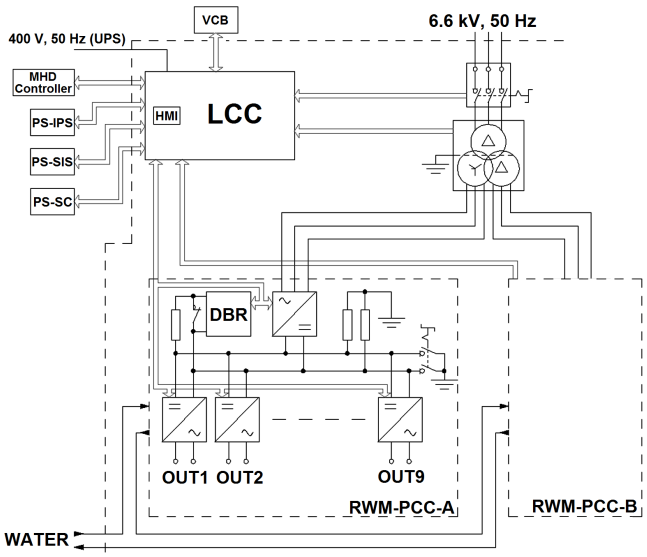

Fig. 2. Overall block diagram of RWM-PS.

critical requirements. After a brief description of the load, the design of the RWM-PS is treated in detail and some conclusions on the present achievements are given.

II. Load Description

The load of the RWM-PS is represented by the 18 RWM-CC. These coils are arranged in three rows in the poloidal direction by 6 in the toroidal one. A set of three coils is represented in Fig. 1. Their dimensions are variable, but typically the side length is about 0.7 m. More technical details on RWM-CC can be found in [6]. Each coil is connected to the RWM-PS with a feeder passing through the cryostat and a coaxial cable. Presently, it is foreseen to install the RWM-PS along the north wall of the JT-60SA experiment building; this allows limiting the cable length in the range 55/88 m (depending on the coil). The length is such that a reasonable voltage drop can be achieved with the selected cross section of 100 mm^2. When not in use or in case of maintenance, each RWM-CC can be isolated from the RWM-PS with a dedicated disconnector (DCDS).

III. Voltage Requirements

The voltage across the RWM-CC necessary to achieve the required current with the specified bandwidth has been calculated in [6], on the basis of the impedance characteristic achieved through the finite-element (FE) analyses carried out in the past years. To these values, the voltage drops across cable and feeder have been added. Assuming some margin, the rated peak current and voltage at the inverter output are set at 300 A and 240 V, respectively. In [6], it has been pointed out that the load impedance increases dramatically with the frequency while it is only few tens of megohms in dc operation, due to the low number of coil turns (only 8). Therefore, also at low constant voltage, the current increases very rapidly: this might represent a concern for the current control system.

In case of fast transients of the plasma current, electromotive forces (EMFs) can be induced in the RWM-CC. The maximum value and duration have been estimated through FE analyses, resulting in 170 V for 15 ms, keeping a significant margin [6]. The RWM-PS shall be able to timely react to this voltage in order to limit the output current overshoot within 90 A, to avoid overstressing the RWM-CC.

To avoid damages on the insulating material of the RWM-CC, the maximum transient peak voltage and the voltage slope at coil terminals have to be limited to ±550 V and 20 MV/s, respectively. These values have been derived from coil design and experience, with additional margins.

IV. Description of the RWM-PS

This section describes the design of the RWM-PS, which has been developed on the basis of the specific requirements of this application.

A. Block Diagram

The block diagram of the RWM-PS is shown in Fig. 2. The system is composed of an ac disconnector, a step-down transformer, two ac/dc rectifiers, 18 water-cooled fast inverters, and a local control cubicle (LCC). The fast inverters are divided in two groups, each fed by one ac/dc converter, fed in turn by a dedicated secondary winding of the step-down transformer. The latter is connected at the primary side to the ac disconnector, which in turn is fed with 6.6 kV_{rms}, 50 Hz through a vacuum circuit breaker (VCB not part of the RWM-PS), which can be opened in case of severe faults.

The dc-link capacitor bank is distributed among the inverters. The combination of nine fast inverters with their dc-link capacitors and the respective ac/dc converter constitutes a subsystem called power conversion cabinet (PCC). The ground reference of the system is provided separately for the two PCCs, with two resistors connected to the dc link.

The choice of dividing the system in two PCCs has been dictated by the layout constraints, as shown in the following. It guarantees also higher system availability and flexibility. A step-down transformer with two secondary windings has been adopted to separate the common-mode (CM) voltages of

TABLE I
MAIN PARAMETERS OF THE RWM-PS

Description	Value
Input ac power voltage	6.6 kV 3-phase 50 Hz
Rated power of the step-down transformer	100 kVA continuous, 300 kVA overload (100 s)
Maximum operation duty	100 s every 1800 s
Number of ac/dc rectifiers	2
Nominal active power of each ac/dc rectifier	100 kW
Nominal dc-link voltage	300 V
Dc-link fluctuations in normal conditions	within -6% ÷ +3%
Dc-link overvoltage in case of max induced voltage pulse in all RWM-CCs	< +15%
Number of fast inverter units	18
Type of control for each inverter	Current Control Loop or Voltage Control (open loop)
Type of reference	Arbitrary
Nominal output voltage of each inverter	240 V
Max peak voltage between coil terminals	±550 V, in transients
Max voltage slope at coil terminals	20 MV/s
Maximum pulsed voltage induced into the load	±170 V for 15 ms
Maximum peak output current of each inverter	300 A (1)
Nominal inverter output current in dc operation	> 100 A
Maximum output current ripple of the inverter	±30 A
Inverter bandwidth of the current at -1 dB	1 kHz, in current control
Inverter bandwidth of the current at -3 dB	3 kHz, in current control
Latency between reference and output voltage	< 50 μs
Accuracy of the load current in steady-state	±12 A, up to 100 Hz
Output voltage/current overshoot with reference step variation	< +15%
Output current overshoot in case of max e.m.f. induced in the RWM-CC	< 90 A

(1) With sinusoidal reference waveform for the maximum operation duty

the two PCCs such to reduce the electromagnetic interference, to reduce the harmonic content of the ac input current, and to avoid mutual couplings of the ac/dc rectifiers through the ac input voltage.

The control system, which supervises all the plant, is interfaced with JT-60SA central control system. In particular, it receives the voltage/current references and sends the measurements to the MHD controller, which is in charge of elaborating the real-time algorithms to control the plasma MHD instabilities. In addition, the LCC is interfaced with the power supply supervising computer (PS-SC), internal protection system (PS-IPS), and safety interlock system (PS-SIS) of JT-60SA, and with the VCB (to command its intervention and monitor its status).

B. Main Parameters

The main parameters of the power supply are listed in Table I. The maximum operation duty corresponds to the maximum duration of the plasma flat-top foreseen in JT-60SA. The power rating of the step-down transformer is 300 kVA for 100 s, which is more than enough for the active power to be dissipated on the loads at full current (300 A–3 dB) at 3 kHz. The reactive power exchanged with the load is provided, instead, by the dc-link capacitors. The nominal dc-link voltage has been chosen so that at 85% of this value, the output voltage required to achieve 300 A–3 dB at 3 kHz can still be produced (considering the maximum duty cycle and the voltage drops on IGBTs and output filters).

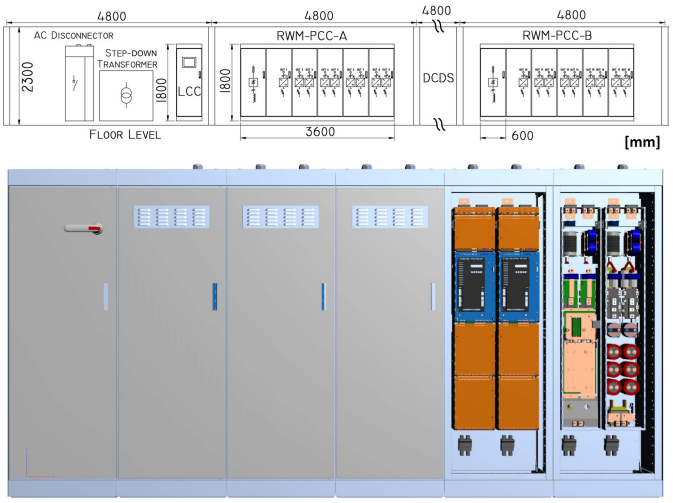

Fig. 3. Overall view of the RWM-PS (top). PCC, with the details of two fast inverters and their internal components on the right (bottom).

C. Layout

The choice of the installation place of the RWM-PS is quite unusual and poses some important constraints on the system layout. To minimize the length of the output cables, the RWM-PS will be installed in three slots of the porch along the north wall of the JT-60SA tokamak building (Fig. 3), each slot being the space between two columns (4.8 m wide). Due to the limited floor capability, all the cabinets will be installed on brackets, and attached to the wall. The power and signal cables will be routed on cable trays on top of the cabinets, while the water cooling pipes will stay below the cubicles. Due to the limited available height of the porch (2.3 m), considering the space required for cable trays and pipes, the maximum height of the cubicles is limited to 1.8 m.

Given these conditions, the selected solution is the following: ac disconnector, step-down transformer, and LCC will be installed in the first slot, while the two PCCs will be distributed in two slots, placed aside a fourth slot hosting the DCDS. This arrangement allows minimizing and equalizing the length of the cables between fast inverters and DCDS. Each PCC is enclosed in a set of six cabinets (600 × 600 mm each): the first contains the ac/dc rectifier and the others host the nine fast inverter modules. This means that one cabinet shall contain two fast inverters (and their dc-link capacitors and output filters), placed side-by-side. The power flow on each inverter module goes from the bottom to the top: two copper busbars provide the input dc power on the bottom, connected to the dc-link capacitor bank; in the middle there is the H-bridge, while the two filters are placed on the top, connected to the output cable. The narrow space available in the cubicles required a careful layout optimization of the fast inverter modules, resulting in the particular elongated shape shown in Fig. 3.

D. Fast Inverter Module

Each fast inverter, with its dc-link filter, capacitor bank, and output filters, is enclosed in a self-contained compact module.

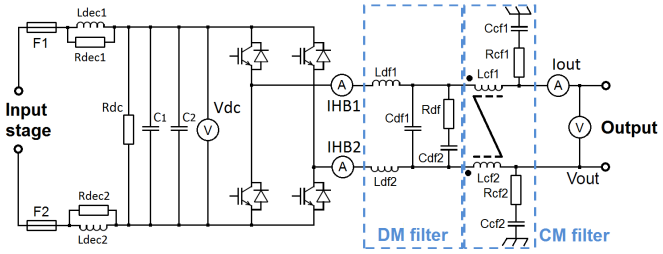

Fig. 4. Simplified scheme of a fast inverter module.

Fig. 5. Fast inverter module.

This facilitates the replacement of the unit, if necessary. Each module is connected at the input to the dc busbar via two fuses, and at the output to the coaxial cable. It has hydraulic connections to the cooling water manifold and signal connections toward the LCC.

A simplified scheme of the module is shown in Fig. 4. Its main components are described in the following. Fig. 5 shows the first fast inverter module manufactured and ready for the factory tests.

E. DC Link

The dc-link capacitor bank of each PCC is divided into nine modules, one for each fast inverter, each connected to the dc busbar through a decoupling *RL* filter. This solution, with respect to a concentrated capacitor bank, gives the following advantages: reduced stray inductance between capacitors and inverters, due to their close proximity; symmetry of the aforementioned stray inductances among the inverters; and reduction of the total number of fuses. Each module consists of six electrolytic capacitors in parallel, each rated for 10 mF and 400 V. The *RL* filter has the main aim of increasing the damping factor of the dc link, in order to reduce the resonance effects among the capacitor modules. In parallel to the electrolytic capacitors, a couple of 220 μF and 800-V low-loss polypropylene film capacitors is installed very close to the fast inverter. Most of the high-frequency current

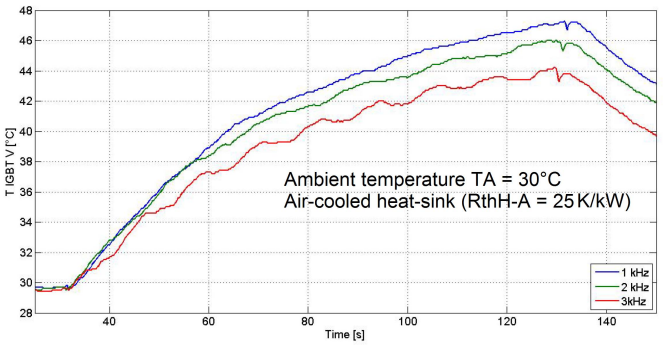

Fig. 6. Internal temperature of a fast inverter power module with air cooling.

generated by the switching of the H-bridge circulates on these film capacitors through a low-inductance path guaranteed by laminated busbars. The lower frequency harmonics will instead circulate mostly on the larger electrolytic bank. This allows reducing the electromagnetic emissions due to the inverter switching operation and guarantees a stable dc-link voltage at the H-bridge terminals.

F. H-Bridge

The H-bridges represent the heart of the RWM-PS. As described in [7], to guarantee the required dynamic performance with a single H-bridge per inverter, a switching frequency of at least 30 kHz has to be adopted, with unipolar pulsewidth modulation (PWM) [9]. This is possible with the technology available today, by adopting fast hybrid Si–SiC power modules, in this case a couple of Infineon FF600R12IS4F. Each of these devices is composed of two silicon IGBTs (1200 V and 600 A), each with an antiparallel SiC diode (1200 V and 360 A), realizing an inverter leg. The SiC diodes, thanks to their reduced reverse recovery effects, show reduced power losses and commutation time; the latter aspect makes it possible to drive the IGBTs with gate resistances of smaller values with respect to conventional Si devices, thus reducing the IGBT switching losses too. Moreover, the dead time can be shortened, thus reducing its negative impact on the converter linearity. Deeply tested with the previous inverter prototype [7], these hybrid components showed high reliability and allowed fulfilling all the dynamic requirements at reasonable cost, thus they have been selected also for the full RWM-PS. Solutions based on full-SiC power MOSFET modules have been considered too, to achieve further space saving and lower power losses, but finally disregarded, due to: higher cost, lower maturity, and lower current rating.

Fig. 6 shows the temperature measured by the internal negative temperature coefficient thermistor of the hybrid IGBT during three pulses (duration 100 s) performed by the previous air-cooled inverter prototype [7], with sinusoidal current reference (300-A peak) at different frequencies. Given the estimated power losses of the H-bridge (1.9 kW), the temperature difference between junction and heat sink has been calculated (16 °C for both IGBT and diode). Combining this value and the experimental data, the expected maximum junction temperature is about 80 °C with ambient temperature

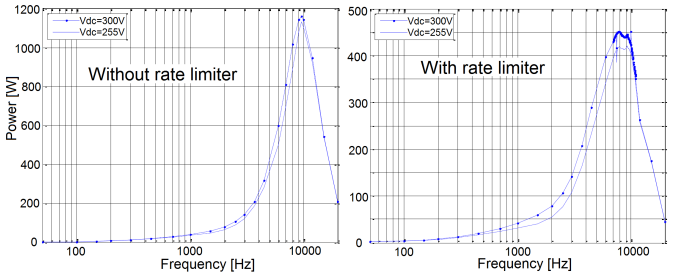

Fig. 7. Power dissipated on the damping resistor of the DM output filter, without and with rate limiter on the sinusoidal current reference (by simulation). Rate limiter set to 6 A/μs.

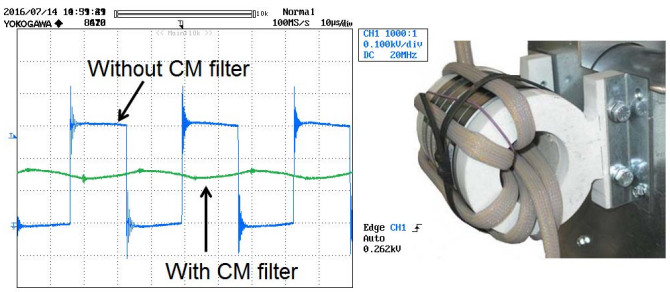

Fig. 8. Voltage measured between one inverter output terminal and negative rail of dc link (left). Prototype of CM filter inductor (right).

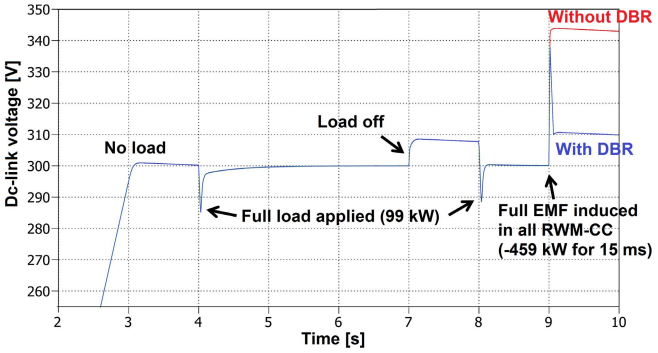

Fig. 9. Simulation of dc-link voltage with the worst load transients.

of 40 °C, well within the limit given by the supplier (125 °C). Similar performance is expected in the final RWM-PS with water cooling cold plate.

G. Differential-Mode Output Filter

A differential-mode (DM) output filter has been introduced in order to reduce the resonances on the long output cable triggered by the steep voltage gradients at inverter output, to reduce the output current ripple, to reduce the current slope in case of short circuits, and to make uniform the load characteristics despite the different cable lengths (more details can be found in [7]). The filter design adopted in the previous inverter prototype has been confirmed also for the final system; the main modification is the new steel grid damping resistor, now rated for a 100-s pulselength. In order to avoid over temperatures on this component in case of input references with frequencies well over the bandwidth, the current control of the first inverter prototype has been improved by introducing a limit on the reference slope. This helps in reducing the power dissipated on the resistor (as shown in Fig. 7), still fulfilling the required bandwidth. Another benefit of the rate limiter on the current reference is the limitation of the voltage slope at coil terminals within 20 MV/s, as required.

H. Common-Mode Output Filter

The chosen modulation technique (unipolar PWM) produces large CM voltage oscillations at the output. In order to reduce the risks associated with electromagnetic emissions on JT-60SA, especially considering the proximity of the output cables and RWM-CC to sensitive diagnostics in the tokamak building, a CM filter has been introduced. (The scheme is shown in Fig. 4.) A prototype has been already built and successfully tested, showing a great reduction of the CM voltage amplitude (Fig. 8).

I. Input Stage

The ac disconnector is air insulated, rated at 7.2 kV and 630 A, and manually operated. Its mechanical life is 3000 cycles, which is sufficient for its purpose, being operated only in case of maintenance.

The step-down transformer has two secondary windings, star and delta connected, each rated at 290 V (no-load). It is enclosed in a dedicated box and natural air cooled.

Each ac/dc rectifier is composed of an incoming three-pole switch fuse, a thyristor rectifier module, a dc-link choke, a surge suppressor, and a dynamic braking resistor (DBR). The fuse provides protection against short circuits and a mean to isolate each PCC from the incoming ac supply. The rectifier module, rated at 350 A, is a six-pulse air-cooled thyristor bridge, based on 1600-V, 216-A power modules IXYS MCC200-16IO1. The current rating has been chosen considering that the maximum output active power of each inverter is 9 kW, which occurs when operated at 3 kHz, with peak current equal to 300 A–3 dB, and loaded with the typical RWM-CC. At the output of each ac/dc rectifier, the 1-mH dc-link choke has the aim to limit the fault current in case of short circuit across the dc link and to reduce the dc current ripple.

The DBR, rated at about 300 A, is a sort of chopper composed of a switching module (containing an IGBT and a voltage clamp circuit) and a braking resistor. Its main purpose is to speed up the discharge of the dc link, in order to: reduce the dc-link overvoltages, facilitate the return into the regulation range, and enhance the capability to cope with repeated events that cause overvoltage (e.g., EMF induced on the RWM-CCs). However, the dc-link capacitor bank is sized so that, also without DBR, the dc-link voltage remains within the specified regulation range of Table I in both normal and abnormal conditions. The DBR is also used to completely discharge the dc link in a few seconds whenever required. However, the safe short circuiting and grounding of the dc link is guaranteed by electromechanical contactor.

Fig. 9 shows the result of a simulation demonstrating the capability of the input stage, with its voltage and current

regulators, to keep the dc-link voltage within the limits of Table I in the worst transient conditions. Here, the ac/dc rectifier is enabled at $t = 0$ and charges the dc link from 0 to 300 V in 3 s. Then, at $t = 4$ s, an ideal 99-kW load step is applied to the dc link (9×11 kW, considering 2 kW of power losses per inverter), resulting in a voltage drop of 5.3%, quickly recovered. At $t = 7$ s, the load is disconnected and the dc-link voltage rises by 2.8%. At $t = 8$ s the full load is reapplied and at $t = 9$ s the load injects 459 kW (9×300 A $\times$ 170 V) for 15 ms into the dc link (simulating the maximum EMF induced in all the RWM-CC). The dc-link voltage rises by 14.7% and 12.7%, with the DBR, respectively, disabled and enabled. Then, with DBR, the dc-link voltage is promptly reduced.

J. Control Hardware

The control section of the RWM-PS is composed of the following elements: the LCC, the PCC control panels, the ac/dc rectifier control boards, and the fast inverter control boards. The LCC includes the PLC, the touch-screen operator panel, and the transformer monitoring unit. The PLC takes care of the slow control and monitoring of the RWM-PS and provides the interfaces with PS-SC (via ethernet), VCB, PS-IPS, and PS-SIS (via digital signals). Through the operator panel, it is possible to set the control parameters, to locally control and monitor the RWM-PS operation and to log the alarms. The two PCC control panels provide the measurements of dc-link voltage and current and a key switch to enable the PCC operation. The rectifier control board provides the following standard main functions: synchronization of the gate pulses with the ac grid, acquisition of the ac and dc measurements, dc voltage and current regulation, and generation of the firing commands for the thyristors.

The fast inverter control board has been developed specifically for this application, due to the very demanding performance required. In fact, it has to provide the high computational power for the fast control algorithms, fast and reliable protections, low latency, and a precise and fast PWM modulator. For these reasons, it includes on the same printed circuit board a fast 32-b dual-core DSP (150 MHz) and a high-end FPGA (500 MHz). The real-time control algorithms are executed at 60 kHz by the DSP, while time critical functions are implemented in the FPGA (averaging of output measurements, fast protections, and dead-time compensation). The exchange of reference and output voltage and current measurements with MHD controller is realized with $\pm$10-V analog signals on shielded twisted-pair cables. The reference is filtered with an analog low-pass filter realized with an instrumentation amplifier and sampled by a 12-b ADC at a rate of 60 ksps. The control board includes also a CAN bus interface for PLC and RS-485 and Ethernet interfaces.

To guarantee the safety of the operators, reinforced insulation is employed between any live circuit and the low voltage control circuit (withstand voltage: $\geq$3 kVac). This is realized by adopting insulated dc power supplies, insulated voltage and current transducers, and proper optocouplers in the control boards.

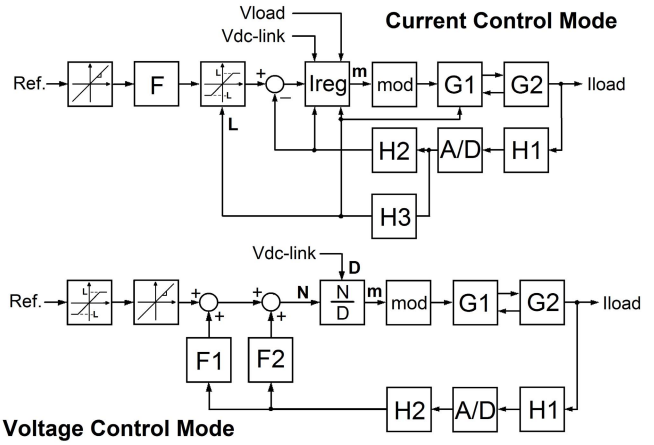

Fig. 10. Simplified block diagrams of fast inverter current and voltage regulators.

K. Real-Time Control Software

The real-time control software of the power converters runs in their control cards. While for ac/dc rectifiers, the performance required is not critical, that for fast inverters required an intense development. Each inverter can be controlled in current control mode (CCM, closed loop) or voltage control mode (VCM, open loop), the choice depending on the experimental needs. With reference to Fig. 10, in CCM the reference (Ref.) passes through the rate limiter and the digital filter F to flatten the response within the bandwidth and attenuate the harmonic components at higher frequencies. The regulator block (Ireg) includes a PI digital regulator and the compensations of the voltage drops on power semiconductors and DM output filter. G1 represents the dead-time compensation, G2 stands for the fast inverter and load, H1 is the current transducer and conditioning, H2 averages the input over a half PWM period, and H3 is the load current limiter. The latter is a function that protects the load and the inverter against temporary overcurrents which could occur in some situations (e.g., in case of EMF induced into the RWM-CC), without permanently stopping the inverter (which could be detrimental to the RWM control). Its working principle is the following: as soon as the load current reaches a user-settable threshold, the FPGA removes the gate commands for a given time and informs the DSP. In some hundreds of microseconds, the load current decays to zero, because the freewheeling diodes apply a counter voltage equal to the dc-link voltage. In the meanwhile, the DSP nullifies the current reference and sets the integrator of the PI regulator to the measured load voltage (to avoid over shoots at restart). As soon as the FPGA reapplies the gate commands, the DSP linearly ramps up the current reference to the incoming reference signal and the current control is reachieved within 1 ms. The sequence is shown in Fig. 11, where the highest EMF (170 V) is assumed to be induced in the RWM-CC while the load current is 300 A; the current overshoot is lower than 90 A, as required. In addition to this load current limiter, standard software and hardwired overcurrent protection are provided (with higher thresholds), to stop permanently the inverter in case of fault (e.g., short circuit of the load).

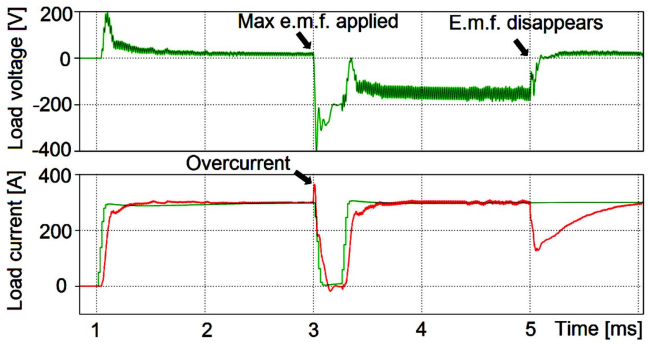

Fig. 11. Simulation of the intervention of the load current limiter in case of EMF induced on the RWM-CC.

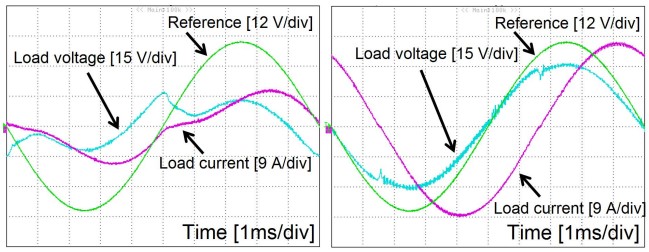

Fig. 12. Load voltage and current without (left) and with (right) dead-time compensation, measured on the first inverter prototype in VCM.

In VCM, the compensations of the voltage drops on IGBTs and output filter (blocks F1 and F2 in Fig. 10) are fundamental to achieve the required accuracy of the voltage control. They are estimated in real time from the load current and the current slope, respectively. For the IGBTs, a model based on a two-slope V–I characteristics has been adopted. Both in CCM and VCM, the compensation of the actual value of the dc-link voltage is implemented too.

After several optimizations carried out on the previous inverter prototype, the minimum dead time to guarantee a safe operation has been found, and it is around 1 μs only. However, due to the high switching frequency, the corresponding voltage error is still unacceptably high (18 V). Thus, it is compensated in real time by a sophisticated algorithm, whose design was complicated by the low impedance of load and the random nature of the reference. Fig. 12 highlights the great impact of the dead-time compensation, with a 100-Hz sinusoidal voltage reference. More details on the compensations can be found in [7].

In VCM, the rated power of the damping resistor of the DM output filter can be exceeded when the voltage reference contains harmonics well over 3 kHz. This problem, discovered during the characterization of the previous inverter prototype [7], has been further studied during the design of the full system. In voltage control, the limitation of the reference slope does not seem a valid solution, because it would cause current distortions and drifts. Therefore, a software thermal protection has been implemented. In detail, the instantaneous power dissipated by the damping resistor is calculated from the load voltage measurement; on this basis, the temperature is estimated through a thermal model and compared with a threshold. The validity of this solution will be verified with experimental tests.

V. Conclusion

To control the RWMs in JT-60SA, a very compact, flexible, and efficient power supply (RWM-PS) has been designed, comprising 18 independent inverters. The very demanding requirements (current bandwidth: 3 kHz, latency 50 μs) are satisfied thanks to the adoption of high-end control hardware, optimized software, and hybrid Si–SiC power IGBTs. These components have been recently introduced in the market and never used before on MHD control applications. During the design and testing of the first inverter prototype in 2014–2016, several design issues related with the fast commutations, the arbitrary reference, and the nature of the load have been solved through a careful layout, an elaborate control system, a DM output filter, and special protections. However, some open points remained, like the power dissipated on the filter damping resistor, the CM disturbances, and the excessive slope of the output voltage in certain conditions. However, during the detailed design of the fully system, also these problems have been addressed and the technical solutions have been identified, together with further optimizations. Therefore, the manufacturing phase of the RWM-PS has been launched. The factory tests will be performed in 2017, while the delivery in Japan is foreseen in September 2018.

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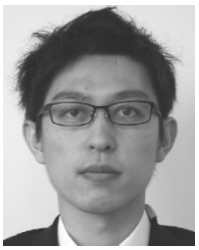

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